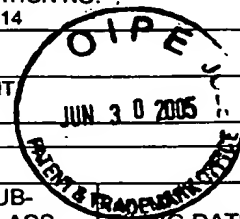


FORM PTO-1449

SECOND SUPPLEMENTAL
INFORMATION DISCLOSURE STATEMENTATTY. DOCKET NO.
1778.0180000APPLICATION NO.
09/925,314FIRST NAMED INVENTOR
Christopher R. RisucciFILING DATE
August 10, 2001ART UNIT
2183

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
12	AA1	3,794,980	02/1974	Cogar <i>et al.</i>			
	AB1	3,811,114	05/1974	Lemay <i>et al.</i>			
	AC1	3,840,861	10/1974	Amdahl <i>et al.</i>			
	AD1	3,983,541	09/1976	Faber <i>et al.</i>			
	AE1	4,110,822	08/1978	Porter <i>et al.</i>			
	AF1	4,149,244	04/1979	Anderson <i>et al.</i>			
	AG1	4,229,790	10/1980	Gilliland <i>et al.</i>			
	AH1	4,295,193	10/1981	Pomerene, James H.			
	AI1	4,432,056	02/1984	Aimura, Harutsugu			
12	AJ1	4,467,409	08/1984	Potash <i>et al.</i>			

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
12	AK1	EP 0 073 424 A2	03/1983	Europe			N/A
	AL1	EP 0 239 081 B1	09/1995	Europe			N/A
12	AM1	EP 0 368 332 B1	09/1997	Europe			N/A

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

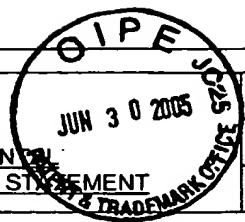
12	AN1	Cobb, Paul, "TinyRISC: a MIPS-16 embedded CPU core," Presentation for Microprocessor Forum, 13 slides (7 pages) (October 22-23, 1996).					
	AO1	U.S. Utility Patent Application No. 09/702,112, inventors Jensen, M., <i>et al.</i> , filed October 30, 2000 (not published) (67 pages).					
	AP1	U.S. Utility Patent Application No. 09/702,115, inventors Jensen, M., <i>et al.</i> , filed October 30, 2000 (not published) (71 pages).					
	AQ1	U.S. Reissue Patent Application No. 10/066,475, inventor Edward Colles Nevill, filed February 1, 2002 (based on U.S. Pat. No. 6,021,265, issued February 1, 2000) (9 pages).					
12	AR1	Preliminary Amendment, filed February 1, 2002, in U.S. Reissue Patent Application No. 10/066,475, inventor Edward Colles Nevill, filed February 1, 2002 (based on U.S. Pat. No. 6,021,265, issued February 1, 2000) (15 pages).					

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DATE CONSIDERED

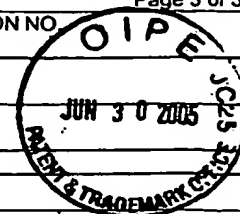
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

FORM PTO-1449 SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT		ATTY. DOCKET NO. 1778.0180000 FIRST NAMED INVENTOR Christopher R. Risucci FILING DATE August 10, 2001	APPLICATION NO. 09/925,314 ART UNIT 2183
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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
125	AA2	4,507,728	03/1985	Sakamoto <i>et al.</i>			
	AB2	4,685,080	08/1987	Rhodes, Jr. <i>et al.</i>			
	AC2	4,724,517	02/1988	May, Michael D.			
	AD2	4,777,594	10/1988	Jones <i>et al.</i>			
	AE2	4,782,441	11/1988	Inagami <i>et al.</i>			
	AF2	5,132,898	07/1992	Sakamura <i>et al.</i>			
	AG2	5,241,636	08/1993	Kohn, Leslie D.			
	AH2	5,327,566	07/1994	Forsyth, Mark A.			
	AI2	5,355,460	10/1994	Eickemeyer <i>et al.</i>			
	AJ2	5,506,974	04/1996	Church <i>et al.</i>			
FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
125	AK2	EP 0 449 661 B1	11/1995	Europe			N/A
	AL2						Yes No
	AM2						Yes No
OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
125	AN2	Gwennap, Linley, "VLIW: The Wave of the Future?: Processor Design Style Could Be Faster, Cheaper Than RISC," <i>Microprocessor Report</i> , Vol. 8, No. 2, pp. 18-21 (February 14, 1994).					
	AO2	Kurosawa, K., <i>et al.</i> , "Instruction Architecture For A High Performance Integrated Prolog Processor IPP," <i>Logic Programming: Proceedings of the Fifth International Conference and Symposium (August 15-19, 1988)</i> , MIT Press, Cambridge, MA, Vol. 2, pp. 1506-1530 (1988).					
	AP2	IBM Technical Disclosure Bulletin, "Patchable Read-Only Storage and Other Patchable Functions," Vol. 27, Issue 6, pp. 3496-3499 (November 1, 1984) (4 pages).					
	AQ2	IBM Technical Disclosure Bulletin, "Patch RAM Load Technique," Vol. 27, Issue 6, pp. 3597-3598 (November 1, 1984) (3 pages).					
	AR2	IBM Technical Disclosure Bulletin, "Microcode Memory Changes," Vol. 21, Issue 1, pp. 341-342 (June 1, 1978) (3 pages).					
EXAMINER					DATE CONSIDERED		
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129	AA3	5,574,873	11/1996	Davidian, Gary G.			
	AB3	5,732,234	03/1998	Vassiliadis <i>et al.</i>			
	AC3	6,266,765 B1	07/2001	Horst, Robert W.			
	AD3	6,272,620 B1	08/2001	Kawasaki <i>et al.</i>			
	AE3	2001/0021970 A1	09/2001	Hotta <i>et al.</i>			
129	AF3	2004/0054872 A1	03/2004	Nguyen <i>et al.</i>			
	AG3						
	AH3						
	AI3						
	AJ3						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
	AK3						Yes No
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	AM3						Yes No

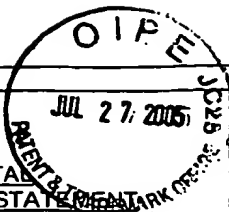
OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

129	AN3	NEC Data Sheet, MOS Integrated Circuit, uPD30121, VR4121 64-/32-Bit Microprocessor (Copyright NEC Electronics Corporation 2000) (76 pages).					
129	AO3	Ross, Roger, "There's no risk in the future for RISC," <i>Computer Design</i> , Vol. 28, No. 22, pp. 73-75 (November 13, 1989).					
129	AP3	NEC User's Manual, VR4100 Series™, 64-/32-Bit Microprocessor Architecture, pp. 1-11 and 54-83 (Chapter 3) (Copyright NEC Corporation 2002).					
	AQ3						
	AR3						

EXAMINER

DATE CONSIDERED

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FORM PTO-1449

ATTY. DOCKET NO.

1778.0180000

APPLICATION NO.

09/925,314

THIRD SUPPLEMENTAL

INFORMATION DISCLOSURE STATEMENT

FIRST NAMED INVENTOR

Christopher R. Risucci

FILING DATE

August 10, 2001

ART UNIT

2183


U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
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	AC1						
	AD1						
	AE1						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
	AL1						Yes No
	AM1						Yes No
	AN1						Yes No
	AO1						Yes No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR1	Case, Brian, "ARM Architecture Offers High Code Density: Non-Traditional RISC Encodes Many Options in Each Instruction," <i>Microprocessor Report</i> , Vol. 5, No. 23, pgs. 11-14 (December 18, 1991).
	AS1	
	AT1	

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